IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Original) A semiconductor integrated circuit comprising:

circuits having a certain function;

a plurality of input terminals which receive input data to said circuits from the outside;

a plurality of output terminals which output data output from said circuits to the outside;

a plurality of first registers connected in series, said plurality of first registers shifting stored data to respective adjacent registers in sequence, and said plurality of first registers being connected in one-to-one correspondence to said plurality of input terminals or to said plurality of output terminals;

a plurality of second registers connected in series, said plurality of second registers shifting stored data to respective adjacent registers in sequence, and said plurality of second registers being connected in one-to-one correspondence to said plurality of input terminals or to said plurality of output terminals;

a first scan input terminal formed at one end of said plurality of first series-connected registers;

a first scan output terminal formed at the other end of said plurality of first series-connected registers;

a second scan input terminal formed at one end of said plurality of second series-connected registers;

a second scan output terminal formed at the other end of said plurality of second series-connected registers; and

an operation control circuit which controls operations of said circuits and said plurality of first and second registers.

Claims 2-20 (Canceled).